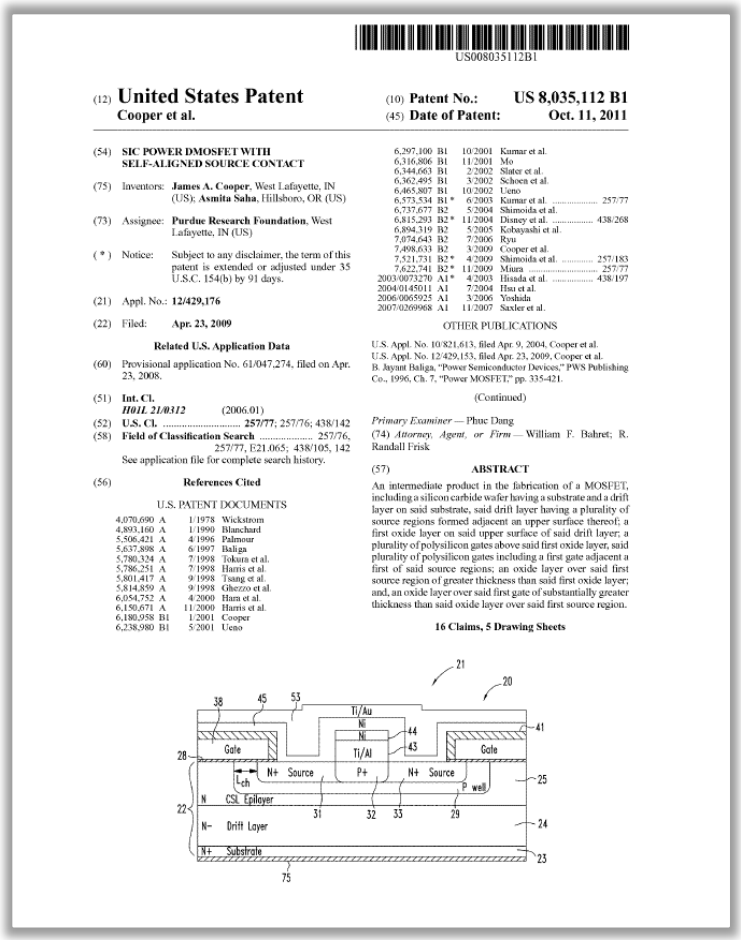
EXHIBIT D

U.S. Patent No. 8,035,112 – STMicroelectronics SCTW90N65G2V



US008035112B1

(12) **United States Patent**
Cooper et al.

(10) **Patent No.: US 8,035,112 B1**
(45) **Date of Patent: Oct. 11, 2011**

(54) **SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT**

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(73) Assignee: **Purdue Research Foundation**, West Lafayette, IN (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.

(21) Appl. No.: **12/429,176**

(22) Filed: **Apr. 23, 2009**

Related U.S. Application Data

(60) Provisional application No. 61/047,274, filed on Apr. 23, 2008.

(51) **Int. Cl.**
H01L 21/0312 (2006.01)

(52) **U.S. Cl.** **257/77**; 257/76; 438/142

(58) **Field of Classification Search** 257/76, 257/77, E21.065; 438/105, 142
See application file for complete search history.

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(Continued)

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(74) *Attorney, Agent, or Firm* — William F. Bahret; R. Randall Frisk

(57) **ABSTRACT**

An intermediate product in the fabrication of a MOSFET, including a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof; a first oxide layer on said upper surface of said drift layer; a plurality of polysilicon gates above said first oxide layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions; an oxide layer over said first source region of greater thickness than said first oxide layer; and, an oxide layer over said first gate of substantially greater thickness than said oxide layer over said first source region.

16 Claims, 5 Drawing Sheets

Title: SIC Power DMOSFET with Self-Aligned Source Contact

Priority Date: April 23, 2008

Filed Date: April 23, 2009

Issued Date: October 11, 2011

Expiration Date: July 23, 2029

Inventors: Cooper, James A., Saha, Asmita

Exemplary Claim: 6

Claim 6

A **mosfet structure**, comprising:

a **(SUB) silicon carbide wafer having a substrate body** with an **(US) upper surface**,

said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;

a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(ST) adjacent said source region**;

(GAT) at least two polysilicon gates above said **(SOX) substrate surface oxidation layer**, said **(GAT) gates** each having a **(TOP) top**, a **(BOT) bottom** and **(SID) sides**, wherein a **(ST) first source region of said at least one source region** is juxtaposed between **(GAT) first and second adjacent gates of said at least two polysilicon gates**;

a **(GOX) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and

a **(ML) material layer** over said **(ST) first source region** and between said **(GOX) gate oxide layers** on said **(SID) sides** of said **(GAT) gates**,

said **(ML) material layer comprising** one of an oxide and a **(ML) metal contact**.

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Claim 6

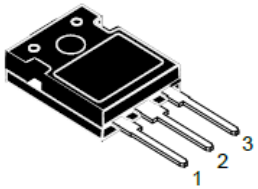
A **mosfet structure**, comprising:

life.augmented

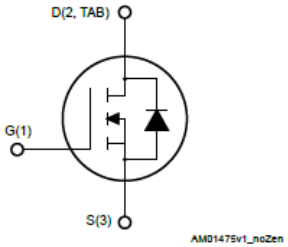
SCTW90N65G2V

Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ., T_J = 25 °C) in an HiP247 package



HiP247



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability (T_J = 200 °C)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

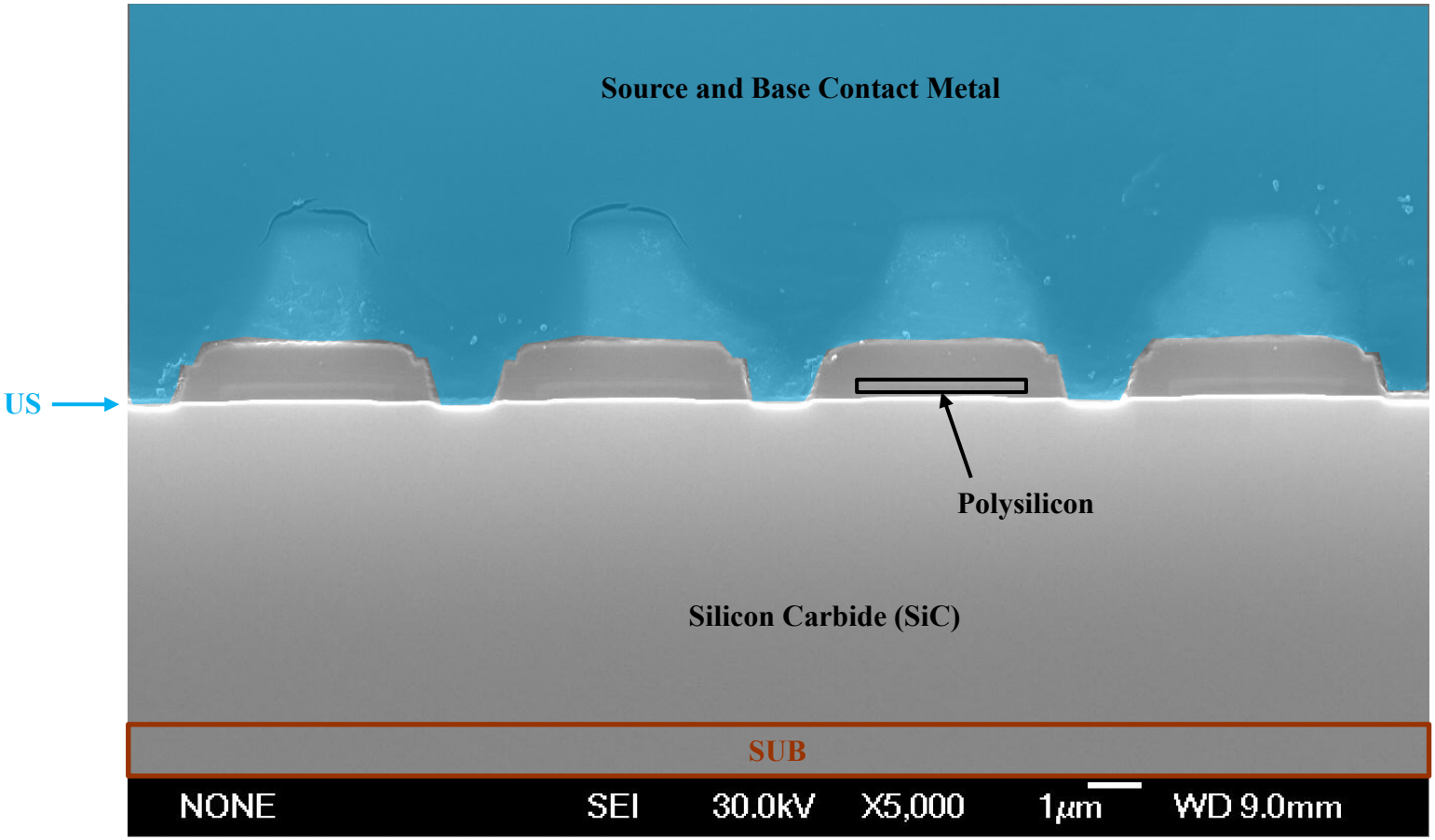
- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

Claim 6

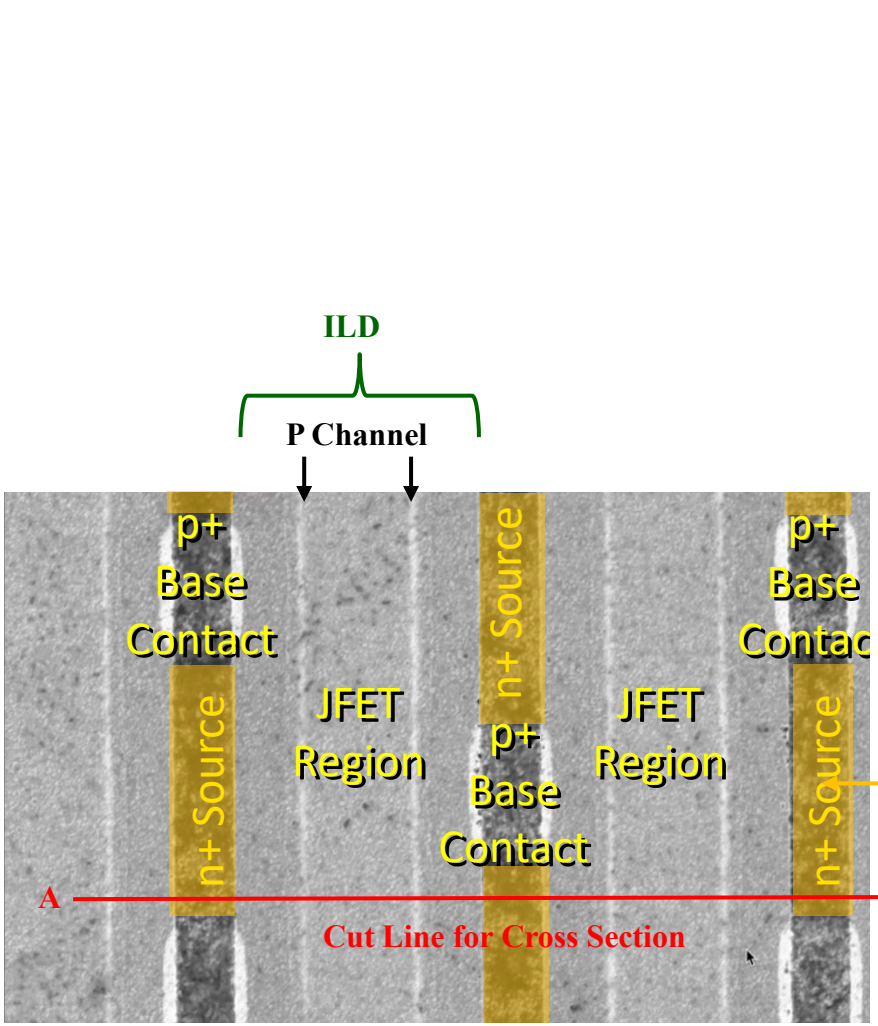
a **(SUB) silicon carbide wafer having a substrate body** with an **(US) upper surface**,

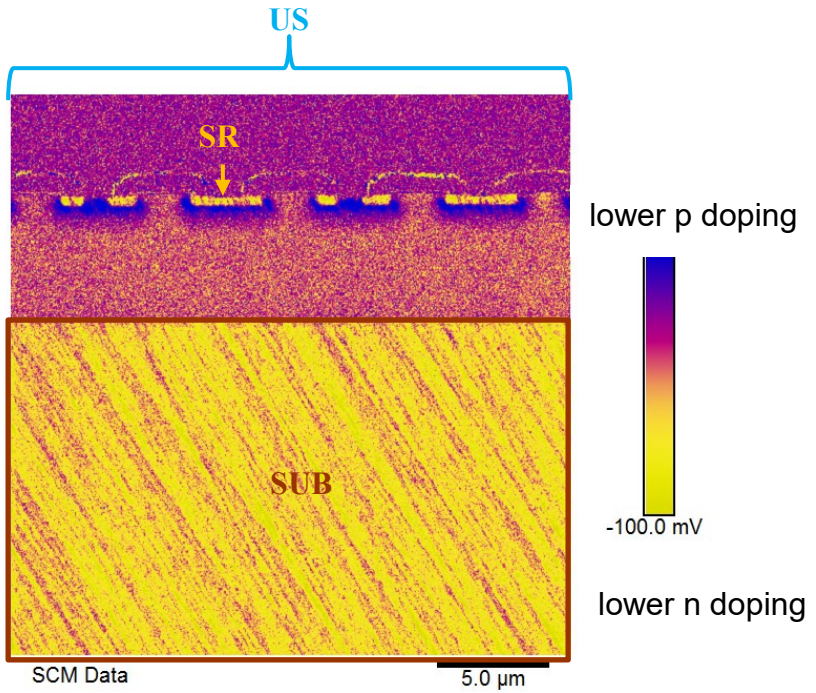


Note: The cross-section SEM above includes silicon carbide, metal, insulators and polysilicon.

Claim 6

said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;

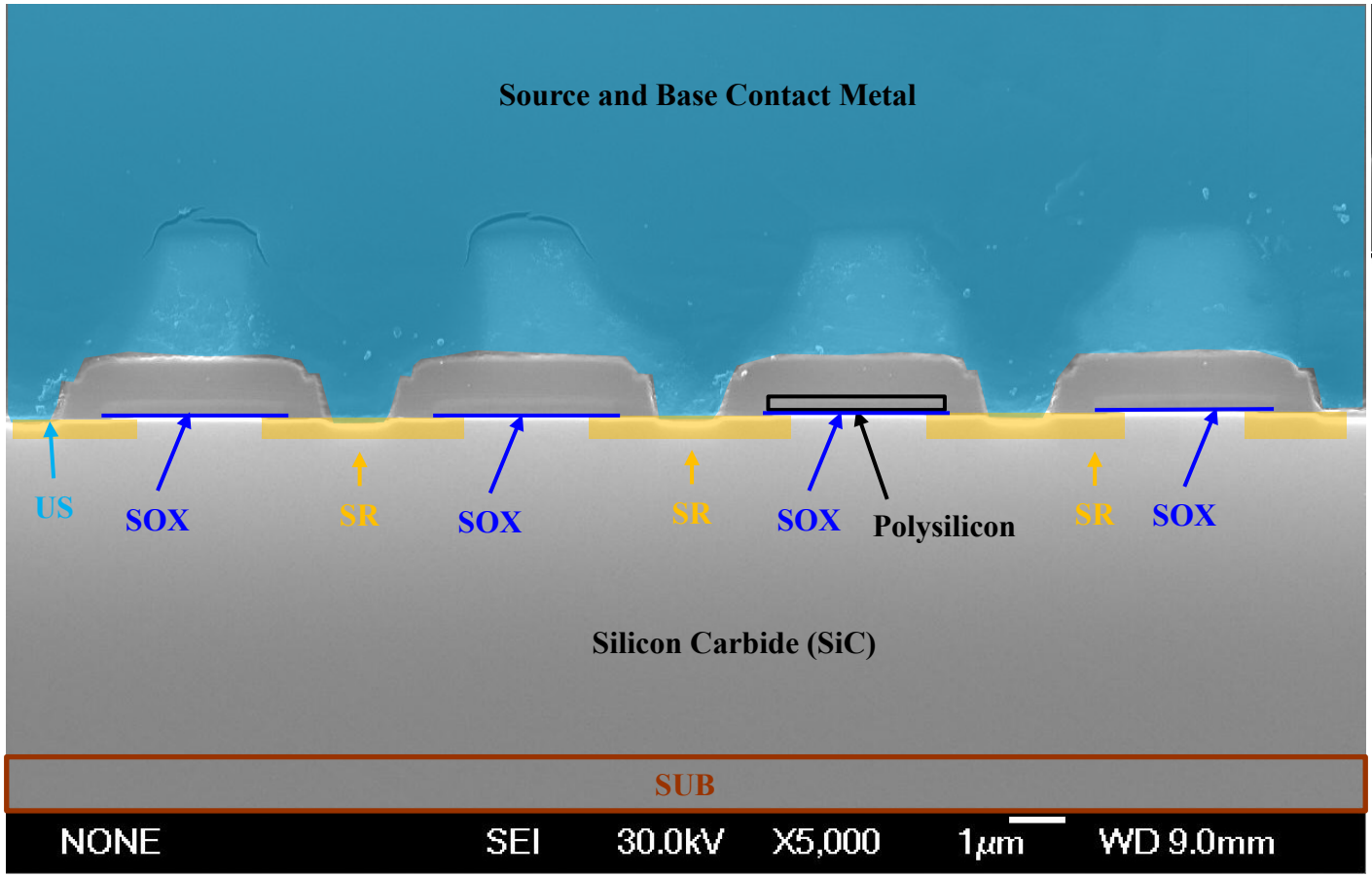


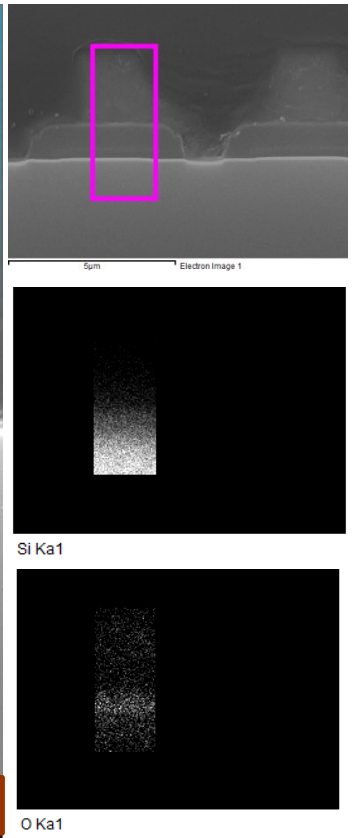


Note: The top down SEM SEPC above has had the top metal layer removed.

Claim 6

a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;



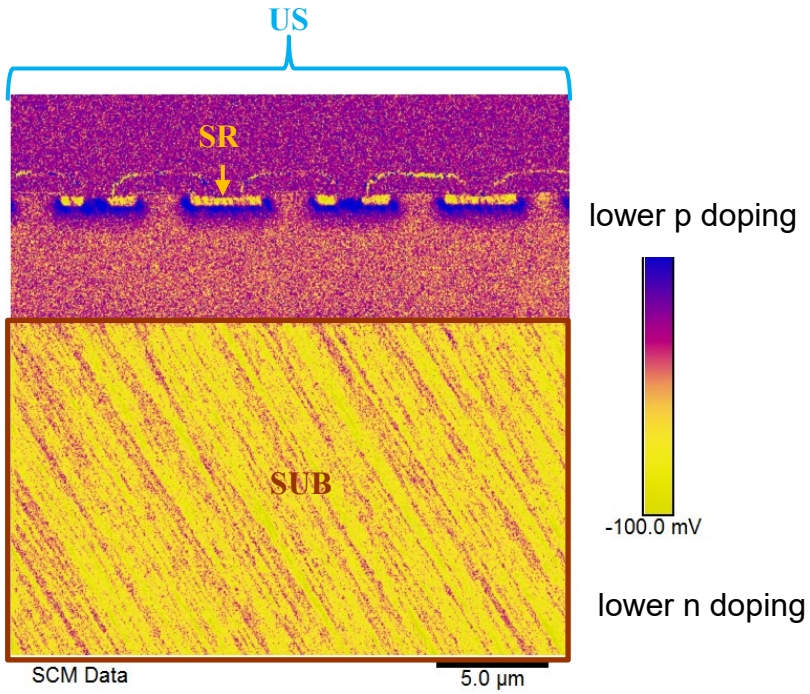


Note: The SEM cross section of the SiC device is shown above.

Note: The elemental maps on the right are shown for the pink box, silicon (Si) and oxygen (O) maps are shown.

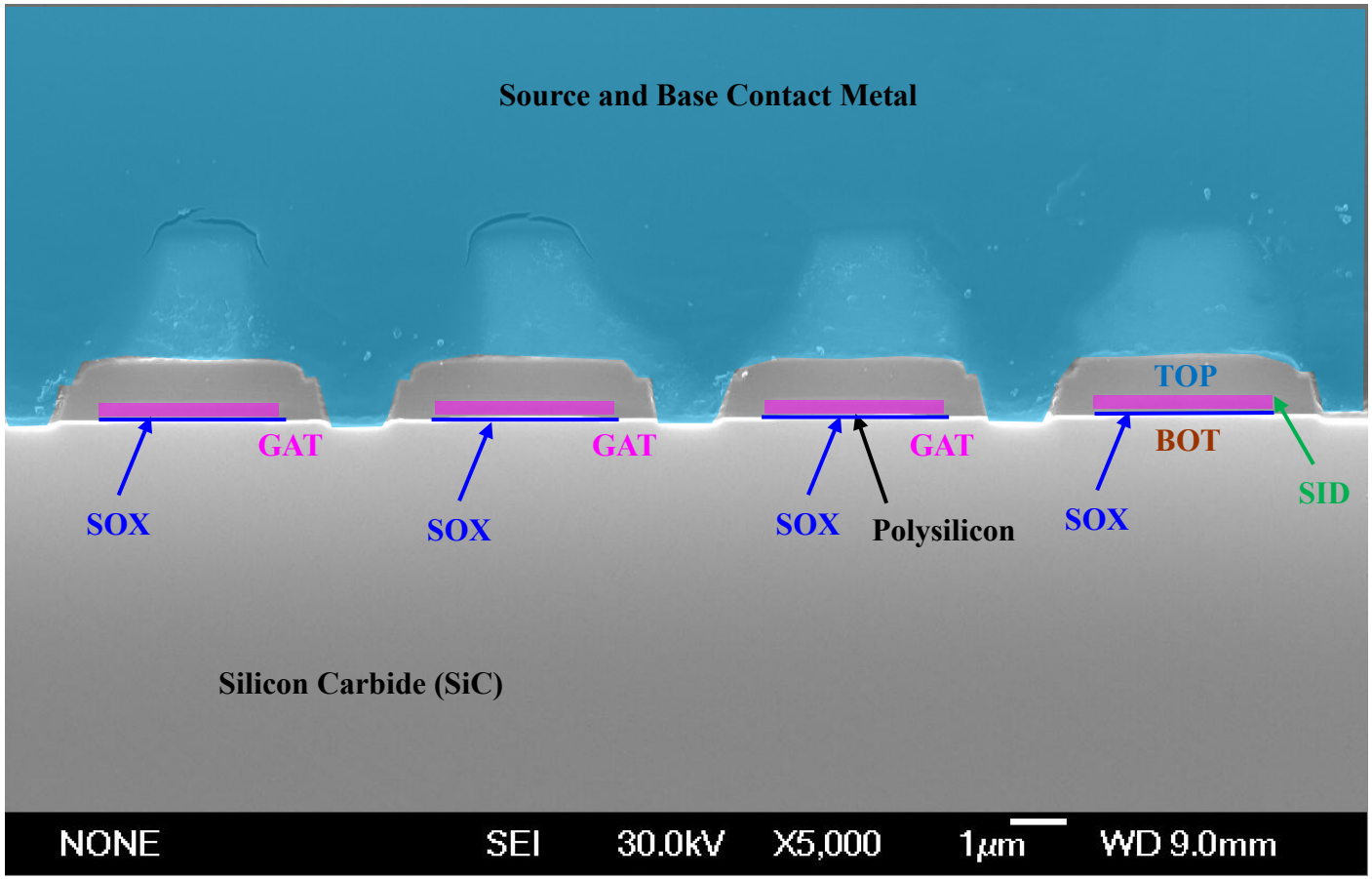
Claim 6

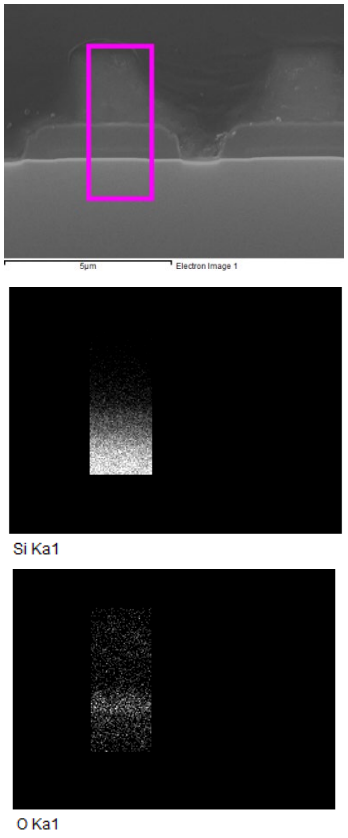
a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;



Claim 6

(GAT) at least two polysilicon gates above said **(SOX) substrate surface oxidation layer**, said **(GAT) gates** each having a **(TOP) top**, a **(BOT) bottom** and **(SID) sides**,



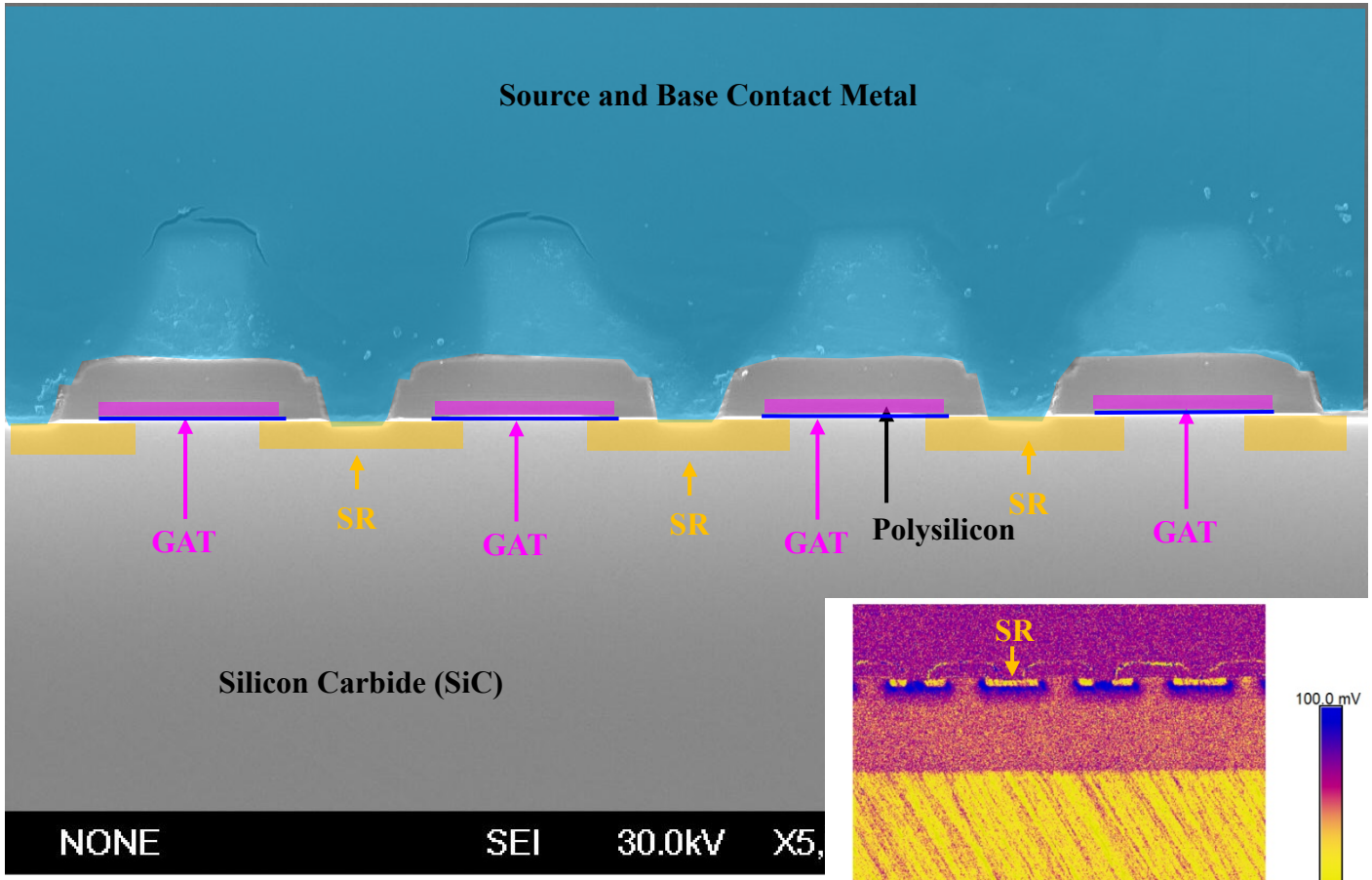


Note: The SEM cross section of the SiC device is shown above.

Note: The elemental maps on the right are shown for the pink box, silicon (Si) and oxygen (O) maps are shown.

Claim 6

wherein a **(SR) first source region of said at least one source region** is juxtaposed between **(GAT) first and second adjacent gates of said at least two polysilicon gates**;



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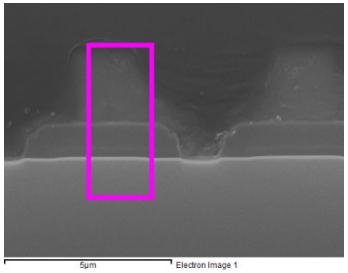
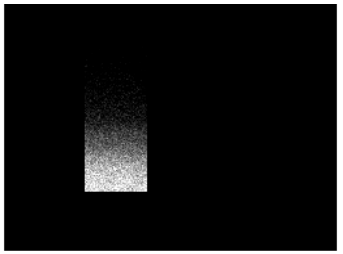
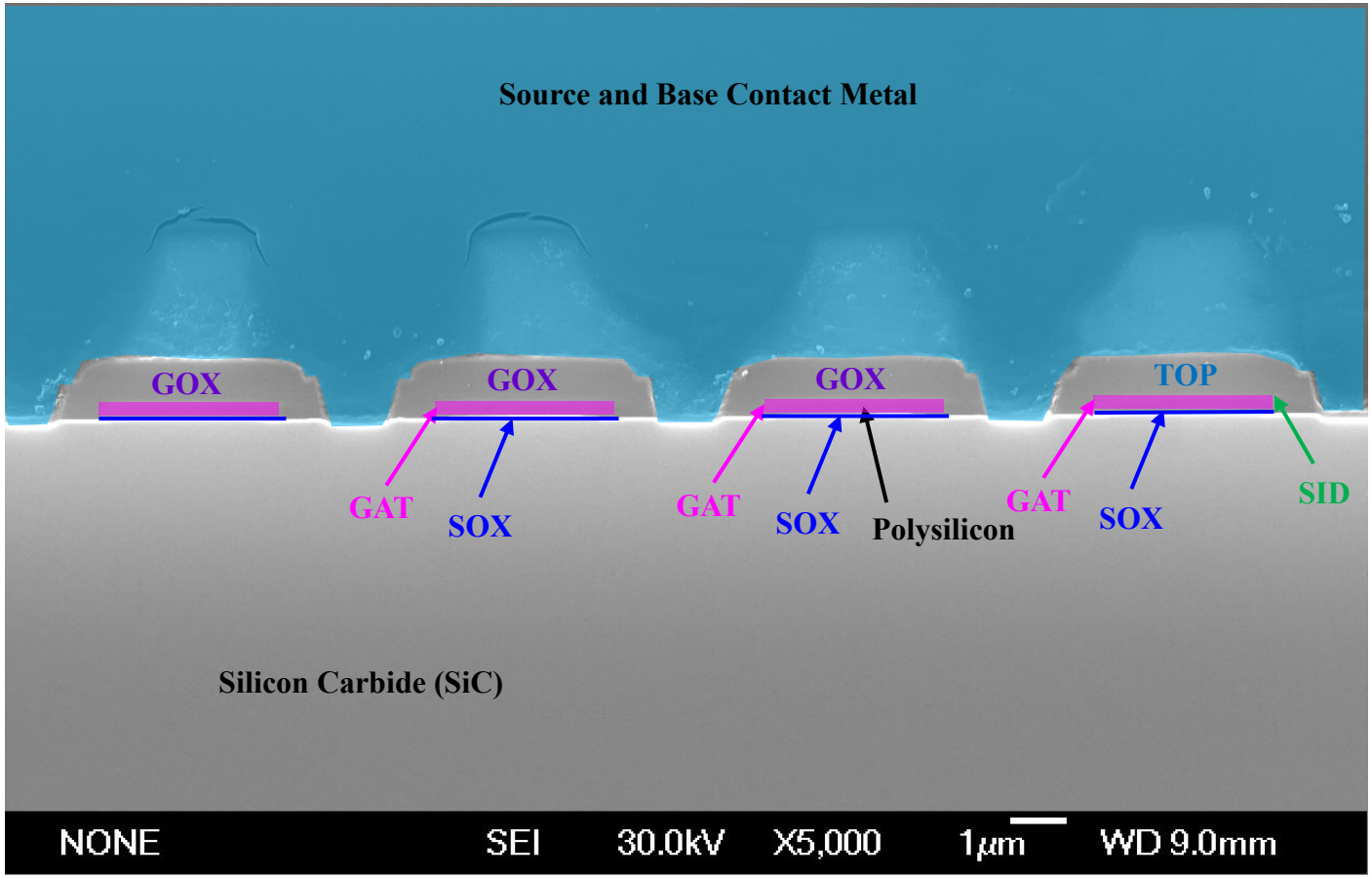


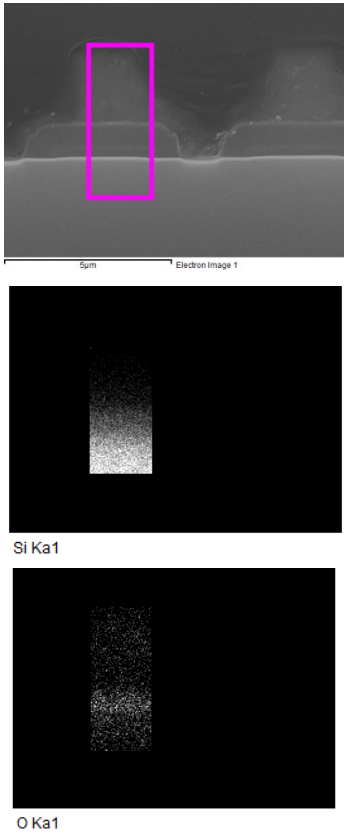


Note: The elemental maps on the right are shown for the pink box, the silicon (Si) map is shown.

Claim 6

a **(GOX) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and





Note: The SEM cross section of the SiC device is shown above.

Note: The elemental maps on the right are shown for the pink box, silicon (Si) and oxygen (O) maps are shown.

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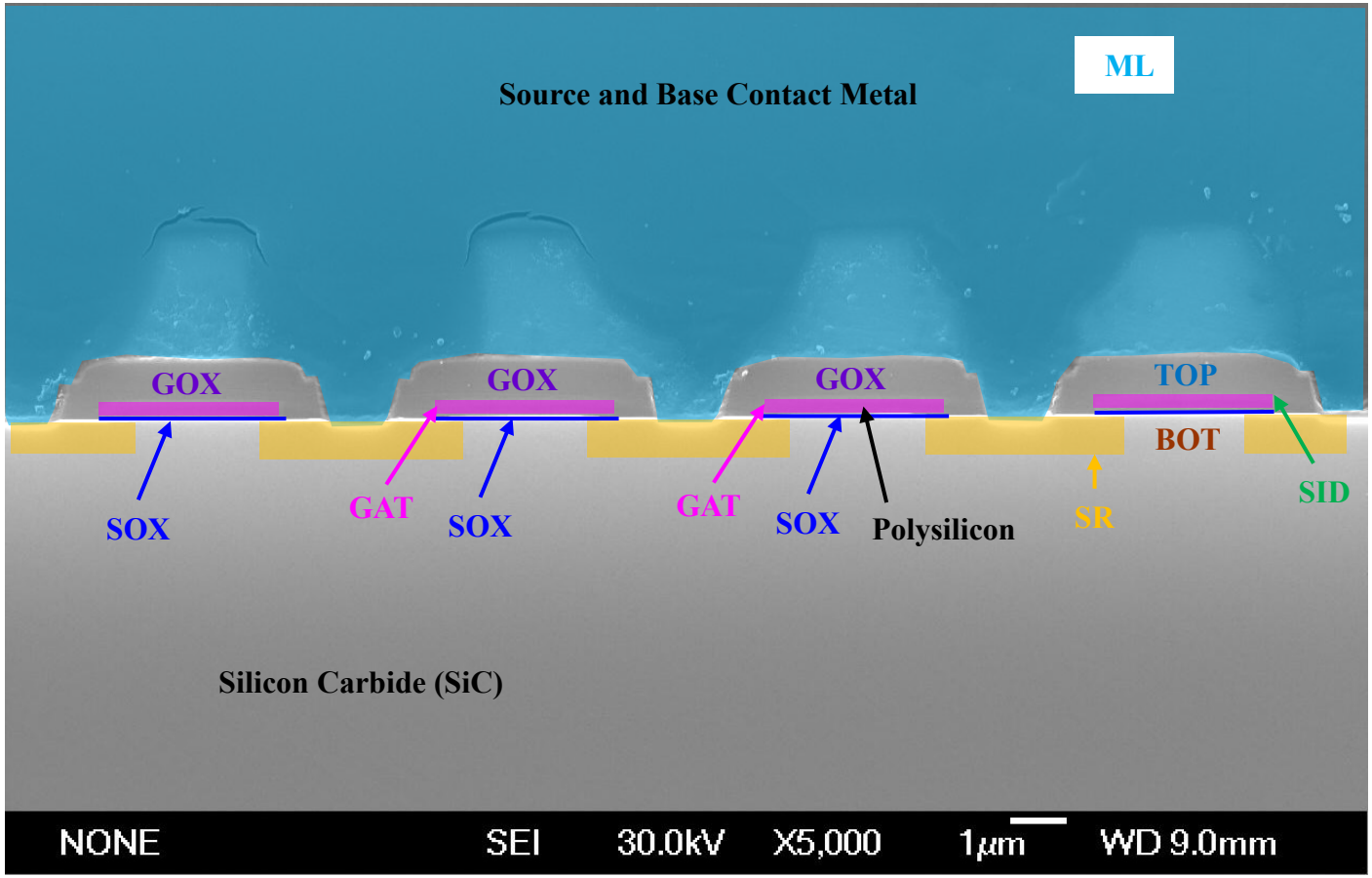
Claim 6

a **(ML) material layer** over said **(SR) first source region** and between said **(GOX) gate oxide layers** on said **(SID) sides** of said **(GAT) gates**, said **(ML) material layer comprising** one of an oxide and a **(ML) metal contact**.



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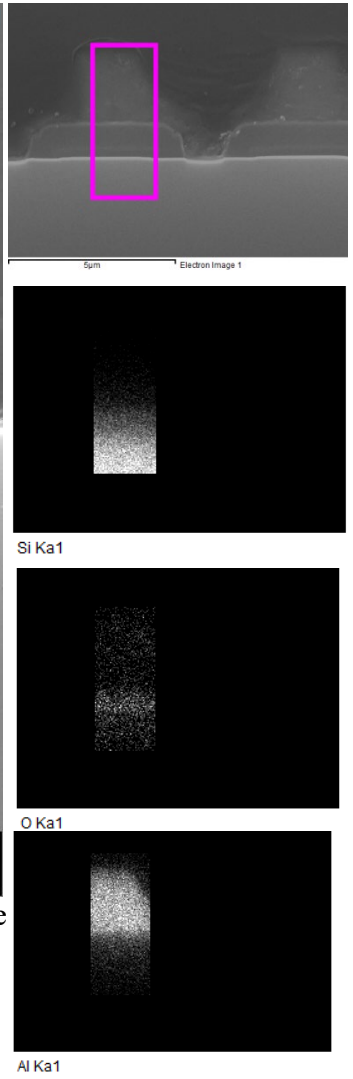

Note: The elemental maps on the right are shown for the pink box, silicon (Si), oxygen (O) and aluminum (Al) maps are shown.